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Micallef, Alexander; Apap, Maurice; Spiteri-Staines, Cyril; Guerrero, Josep M.

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# Selective Virtual Capacitive Impedance Loop for Harmonic Voltage Compensation in Islanded MicroGrids

Alexander Micallef, Maurice Apap and Cyril Spiteri-Staines
Department of Industrial Electrical Power Conversion
University of Malta
Msida. MSD 2080. Malta.
Email: alexander.micallef@um.edu.mt

Josep M. Guerrero
Department of Energy Technology
Aalborg University, Denmark
Email: joz@et.aau.dk

***Abstract*—Parallel inverters having LCL output filters cause voltage distortions at the point of common coupling (PCC) in islanded microgrids when non-linear loads are present. A capacitive virtual impedance loop could be used to provide selective harmonic compensation in islanded microgrids, instead of introducing additional active or passive filters into the system that could compromise the stability of the microgrid. However, the performance of these compensation loops becomes degraded when a virtual resistance is introduced with the aim to improve the overall stability of the parallel inverters. With the capacitive virtual impedance, there is effectively a compromise between the additional stability provided by the virtual resistance and the harmonic compensation due to the virtual capacitance. This paper focuses on overcoming this limitation of the capacitive virtual impedance with additional virtual resistance for selective harmonic compensation in islanded microgrids. Simulation results were given to show the suitability of the proposed algorithms in reducing the voltage harmonics at the PCC.**

***Index Terms*—microgrids, droop control, voltage harmonics, harmonic compensation, islanded operation, capacitive virtual impedance**

## I. Introduction

In islanded operation, traditional droop control enables the decentralized regulation of the local voltage and frequency of the microgrid by the microsource inverters and also the control of the real and reactive power output of each inverter [1]–[6]. However, microsource inverters with LCL output filters connected to the microgrid have a small inertia when operating as an island and effectively form a weak grid. Harmonic currents drawn by any non-linear loads distort the voltage at the point of common coupling (PCC) due to the voltage drop across the grid side inductors of microsource inverters. These harmonics may cause stability problems due to resonances present on the microgrid [7].

Therefore, harmonic damping techniques must be considered to reduce the voltage distortion by installing either passive or active filters to compensate selected harmonic frequencies [7]. However, these filters can increase resonance problems or may compromise the stability of the islanded microgrid. Instead of using these traditional harmonic compensation techniques, control strategies can be added to the inverters connected to the microgrid to improve the power quality [7] .

A capacitive virtual impedance loop was proposed in [8] to selectively dampen the harmonics at the PCC, which does not introduce any additional passive or active filters into the microgrid. The basic principle of the capacitive virtual impedance loop is to compensate for the non-linear inductive voltage drop across the grid side inductance by introducing a voltage which is equal in magnitude but has an opposite phase shift. Effectively the output voltage of the inverter is distorted to reduce the harmonic output current thus also reducing the voltage distortion after the filter. A resistive virtual impedance component is typically included so as to improve the power sharing between the micro-sources and the stability of the microgrid [4], [9]–[11]. However as shall be described in this paper, the resistive virtual impedance acts on all the frequencies and reduces the effectiveness of the virtual capacitive impedance described in [8].

This paper focuses on the use of a capacitive virtual impedance to achieve attenuation of the harmonics at the PCC. In Section II, a description of the considered microgrid setup and control structure is given. Section III contains a detailed analysis of the capacitive virtual impedance loop. Section IV contains a summary of the simulation results showing the suitability of the proposed algorithm in improving the performance of the islanded microgrid.

## II. Hierarchical Microgrid Architecture

The simulated microgrid setup, shown in the block diagram of Fig. 1, consists of two parallel inverters each with an LCL output filter. A local non-linear load, consisting of a single phase rectifier with smoothing capacitor, was connected to the microgrid through switch S2. For islanded operation, the static switch (SS) is open and the inverters operate autonomously to regulate the local grid voltage and frequency. Switch S1 at the output of inverter 2 allows for synchronization of the inverter via a PLL to the voltage at the PCC, before it is connected to the microgrid, to minimize the transients that occur. The

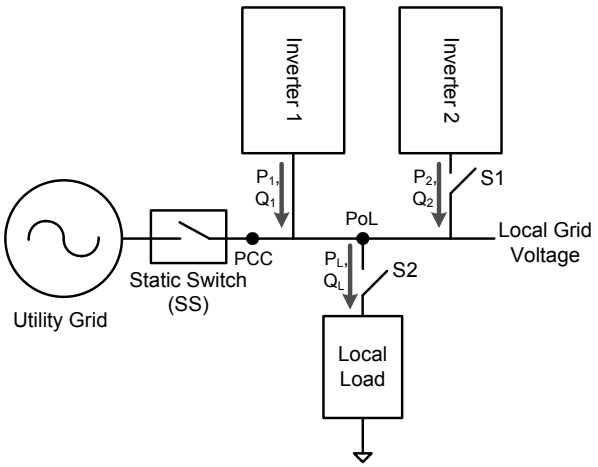



Fig. 1. Block diagram of the microgrid setup.

power lines connecting the inverters to the local grid were represented via the short transmission line model.

### A. Outer Droop Control Loop

In islanded mode, the inverters autonomously regulate the voltage and frequency of the microgrid. Real power is supplied to the loads by using real power against frequency $(P-\omega)$ droops while the reactive power is supplied to the loads by using reactive power against voltage $(Q-E)$ droops. The inputs to the droop controller are the real and reactive power measurements determined from the capacitor voltage ($V_c$) and the grid side inductor current ($i_L$). The voltage reference at the output of the inverter is then determined by the droop control algorithm and input to the inner control loops. The block diagram of the primary control loops implemented in the microsource inverters for islanded operation is illustrated in Fig. 2. Considering that $G_q(s)$ and $G_p(s)$ are the droop controller transfer functions, the droop control functions in islanded mode can be mathematically expressed as:

$$\omega = \omega^* - G_p(s)(P - P^*) \tag{1}$$

$$E = E^* - G_q(s)(Q - Q^*) \tag{2}$$

where P is the real power output of the microsource; Q is the reactive power output of the microsource; $G_p(s) = sm_d + m$ and $G_q(s) = sn_d + n$ are the real and reactive power droop controllers where m and n are the $P-\omega$ and $Q-E$ droop gains and $m_d$ and $n_d$ are the $P-\omega$ and $Q-E$ derivative gain terms. In islanded mode $P^*$ and $Q^*$ are set to zero since the real and reactive power output of the inverters is determined by the local load. The gains of the outer loop controllers are typically defined to achieve minimal deviations from the nominal values of E and $\omega$ while achieving a satisfactory response in the regulation of both the real and reactive powers. The droop gains for the inverters operating in the islanded microgrid, denoted by $m_n$ and $n_n$ from (1) and (2) respectively (where the subscript n is an integer denoting an inverter in the microgrid), are typically related to the maximum power ratings of the inverters.

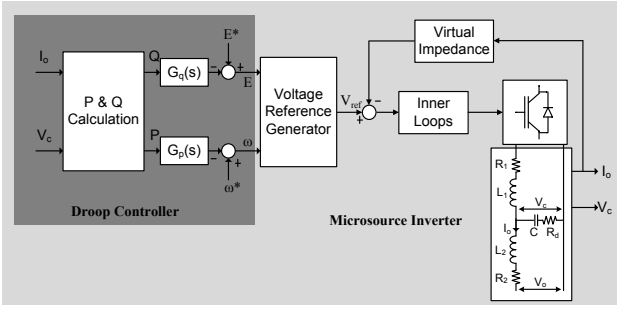



Fig. 2. Block diagram of the inverter primary control loops.

### B. Inner Control Loops

The voltage reference waveform synchronized to the microgrid voltage, if available, is then generated from the output of the droop control functions. The inner controllers that were considered for the single phase inverters, consist of a voltage loop and an inner current loop. Both control loops are based on the stationary reference frame and Proportional-Resonant (PR) controllers [12], [13] were used for both loops. The transfer functions of the voltage and current controllers can be given by [8], [12]:

$$G_V(s) = K_{pV} + \sum_{h=1,3,5,7,9} \frac{k_{iVh}s}{s^2 + \omega_{cVh}s + \omega_h^2} \tag{3}$$

$$G_I(s) = K_{pI} + \sum_{h=1,3,5,7,9,11,13} \frac{k_{iIh}s}{s^2 + \omega_{cIh}s + \omega_h^2} \tag{4}$$

where $K_{pV}$ and $K_{pI}$ are the proportional gains, $k_{iVh}$ and $k_{iIh}$ are the harmonic resonant gains, $\omega_{cVh}$ and $\omega_{cIh}$ determine the harmonic resonant bandwidth and $\omega_h$ is the resonant frequency where $\omega_h = h\omega$ and hence depend on the frequency droop. The PR transfer functions for the voltage and current controllers, (3) and (4) respectively, are obtained from the non-ideal PR transfer function [12]. The term h=1 in (3) and (4) represents the fundamental frequency $\omega$ of the controller that is determined by the droop control algorithm. In addition, selective harmonic control for the $3^{rd}$ up to the $13^{th}$ current harmonic was included so as to provide closed loop control of the selected harmonics within the bandwidth of the inner control loops. Similarly, selective harmonic control for the $3^{rd}$ up to the $9^{th}$ voltage harmonic was included so as to provide voltage regulation of the harmonics compensated by the virtual impedance loop.

A linear block diagram of the inner control loops is shown in Fig. 3 where $V_{ref}$ is the voltage reference that is obtained from the outer droop control loop, $i_L$ is the current through inductor $L_1$, $i_o$ is the current through inductor $L_2$ and $R$ is the damping resistance. The damping resistor, R, was included to reduce the selectivity of the LCL output filter. The closed loop transfer function (CLTF) of the block diagram in Fig. 3 can be expressed by:

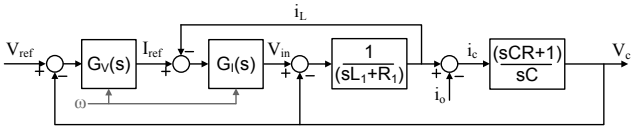



Fig. 3. Block diagram of the inner control loops. $L_1$ is the inverter side inductance, C is the filter capacitance, $R_1$ is the inverter side choke resistance and R is the damping resistance.

$$V_C = \frac{G_I(s)G_V(s)Z_C(s)}{Z_C(s)+Z_L(s)+G_I(s)+G_I(s)G_V(s)Z_C(s)}V_{ref}(s) - \frac{Z_C(s)(Z_L(s)+G_I(s))}{Z_C(s)+Z_L(s)+G_I(s)+G_I(s)G_V(s)Z_C(s)}i_o(s) \quad (5)$$

where $Z_L(s) = sL_1 + R_1$ and $Z_C(s) = (sCR+1)/sC$. The bode plot of the voltage CLTF $\frac{V_C(s)}{V_{ref}(s)}$ for the inner loops with and without the selective harmonic control is shown in Fig. 4. In both cases, the inner loops exhibit a closed loop bandwidth of 900Hz while, as expected, the main difference lies in the fact that the selective harmonic control introduces bandpass characteristics at the desired harmonic frequencies. Fig. 5 shows how the voltage harmonics at the PCC are affected when selective harmonic control is included in the inner loops when the two inverters are operating in parallel as an island. The voltage THD at the PCC was reduced from 4.62% to 3.36% and this reduction can be attributed to the improved harmonic current sharing that results due to the additional selective harmonic control. The reactive current that flows between the inverters is effectively minimized thereby reducing the harmonic current output of the inverters. Therefore, the voltage at the PCC exhibits lower harmonic voltages due to the reduction in the voltage drops across the grid side inductors.

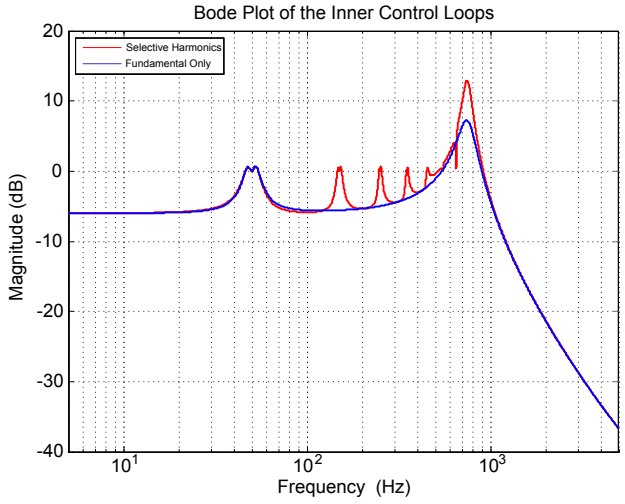



Fig. 4. Bode plot of the inner control loops with and without the selective harmonic control. The PR controller gains that were used in the simulations are: $K_{pV}$ = 0.5, $K_{pI}$ = 2, $k_{iVh}$ = 200/h, $k_{iIh}$ = 200/h, $\omega_{cVh}$ = 0.001$\omega_h$, $\omega_{cIh}$ = 0.001$\omega_h$ and h is the harmonic number. Hardware parameters for inverter 1 were considered for these plots as given in Table I.

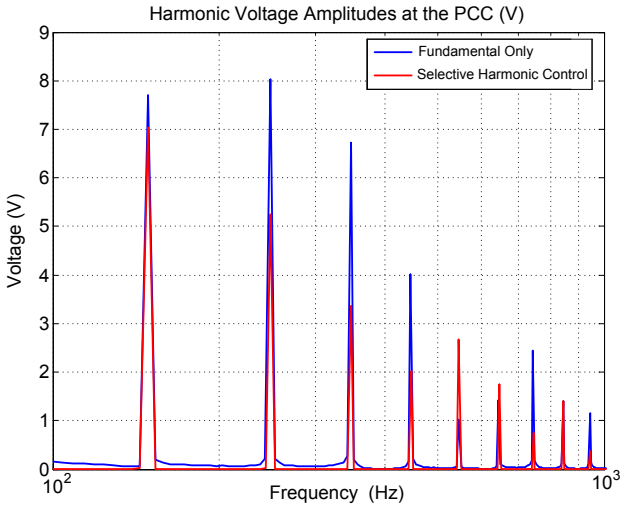
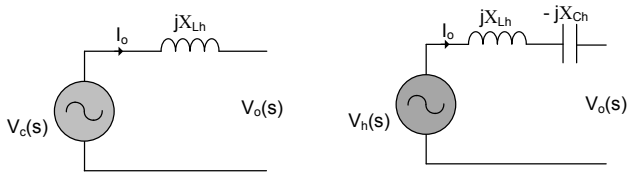



Fig. 5. Comparison of the voltage harmonics at the PCC with and without the selective harmonic control when both inverters are connected to the microgrid. A single phase rectifier with smoothing capacitor load ($L_p = 84\mu H$, $C_p = 235\mu F$ and $R_p = 100\Omega$) was used for these results.

## III. Capacitive Virtual Impedance Loop

A capacitive virtual impedance loop was proposed in [8] with the aim to improve the voltage harmonic distortion at the PCC. The basic principle of the capacitive virtual impedance loop is to compensate for the non-linear inductive voltage drop across the grid side inductance $X_{Lh}$ by introducing a voltage across a virtual capacitive impedance $X_{Ch}$ which is equal in magnitude but has an opposite phase shift. The simplified Thevenin's equivalent circuit of the inverter with an LCL output filter is shown in Fig. 6a while the simplified Thevenin's equivalent circuit of the inverter with an LCL output filter with the proposed capacitive virtual impedance is shown in Fig. 6b. The output voltage of the inverter $V_c(s)$ is effectively distorted to reduce the distortion of the voltage after the filter $V_o(s)$. The block diagram of Fig. 7 shows how the virtual impedance loop interacts with the inner control loops of the inverter. From this figure, the voltage across the capacitor of the output filter can now be expressed by:




(a) (b)

Fig. 6. The capacitive virtual impedance concept. a) Simplified Thevenin's equivalent circuit of the inverter with an LCL output filter. b) The proposed virtual impedance based on the cancellation of the effect of the inductive impedance $X_{Lh}$ by the introduction of a virtual impedance $X_{Ch}$

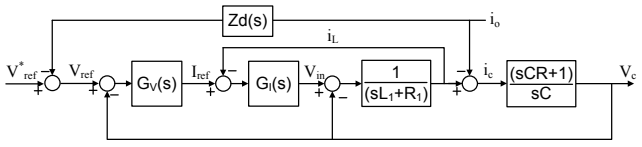



Fig. 7. Block diagram of the inner loops with the additional virtual impedance transfer function $Z_d$(s).

$$V_{ref}(s) = V^*_{ref}(s) - i_o(s)Z_d(s) \tag{6}$$

where $V^*_{ref}(s)$ is the reference voltage that is determined by the outer droop control loop, $V_{ref}(s)$ is the input to the inner loops which includes the additional harmonic voltages and $Z_d$(s) is virtual impedance transfer function. From [8], the virtual impedance transfer function $Z_d$(s) consists of a series of band-pass filters, tuned at each harmonic frequency that is required to be dampened ($3^{rd}$, $5^{th}$, $7^{th}$, and $9^{th}$), cascaded with a capacitive impedance block. $Z_d$(s) can be expressed by:

$$Z_d(s) = \sum_{h=3,5,7,9} \frac{\omega_{ch} k_{Ch}}{s^2 + \omega_{ch} s + \omega_h^2} \tag{7}$$

where $k_{ih}$ are the harmonic resonant gains, $\omega_{ch}$ are the harmonic resonant bandwidths, $\omega_h$ is the $n^{th}$ harmonic frequency and $k_{Ch}$ is the gain at the $n^{th}$ harmonic. Assuming that the bandwidth $\omega_{ch}$ at the $n^{th}$ harmonic frequency is determined such that the interaction with the adjacent harmonics is negligible, then the magnitude and phase contribution of $Z_d$(s) at each of the $n^{th}$ harmonic frequencies can be designed by considering the effect of each harmonic separately to determine the controller gains and then substituting in (7). $Z_d$(s) at the $n^{th}$ harmonic can be denoted by:

$$Z_d(s) = \frac{\omega_{ch} k_{Ch}}{s^2 + \omega_{ch} s + \omega_h^2} \tag{8}$$

Substituting for s = j$\omega$:

$$Z_d(\omega) = \frac{\omega_{ch} k_{Ch}}{j\omega_{ch}\omega + (\omega_h^2 - \omega^2)} \tag{9}$$

The gain $k_{Ch}$ can be determined by from the magnitude of (9) at $\omega$ = $\omega_h$:

$$|Z_d(\omega)|_{\omega=\omega_h} = \frac{k_{Ch}}{\omega_h} \tag{10}$$

where $|Z_d(\omega)|_{\omega=\omega_h}$ is equal to the magnitude of the impedance of the grid side inductance at the $n^{th}$ harmonic frequency. From (9), the phase angle at $n^{th}$ harmonic frequency is $-90^o$.

### *A. Effect of the Resistive Virtual Impedance on $Z_d$(s)*

A resistive virtual impedance $R_V$ is typically included so as to improve the stability of the microgrid and the power sharing between the micro-sources [4], [9]–[11]. $Z_d$(s) can now be described by:

$$Z_d(s) = R_V - \sum_{h=3,5,7,9} \frac{\omega_{ch} k_{Ch}}{s^2 + \omega_{ch} s + \omega_h^2} \tag{11}$$

where $R_V$ acts on all the frequencies and thereby effects the magnitude and phase of the band pass filters determined in (7). Assuming that the bandwidth $\omega_{ch}$ at the $n^{th}$ harmonic frequency is determined such that the interaction with the adjacent harmonics is negligible, then the magnitude and phase contribution of $Z_d$(s) at each of the $n^{th}$ harmonic frequencies can be designed by considering the effect of each harmonic separately to determine the controller gains and then substituting in (11). $Z_d$(s) at the $n^{th}$ harmonic can be denoted by:

$$Z_d(s) = R_V - \frac{\omega_{ch} k_{Ch}}{s^2 + \omega_{ch} s + \omega_h^2} \tag{12}$$

Substituting for s = j$\omega$:

$$Z_d(\omega) = \frac{jR_V\omega\omega_{ch} + (R_V\omega_h^2 - \omega_{ch}k_{Ch} - R_V\omega^2)}{j\omega\omega_{ch} + (\omega_h^2 - \omega^2)} \tag{13}$$

The gain $k_{Ch}$ can be determined from the magnitude of (13) at $\omega$ = $\omega_h$:

$$|Z_d(\omega)|_{\omega=\omega_h} = \frac{\sqrt{(\omega_h R_V)^2 + k_{Ch}^2}}{\omega_h} \tag{14}$$

From (13), the phase angle at $n^{th}$ harmonic frequency is given by:

$$\angle Z_d(\omega)_{\omega=\omega_h} = \tan^{-1}\left(\frac{-R_V\omega_h}{k_{Ch}}\right) - 90^o \tag{15}$$

From (14) and (15) one can conclude that a compromise exists between the phase angle and the magnitude at the $n^{th}$ harmonic. The addition of the resistive virtual impedance component reduces the effectiveness of the capacitive virtual impedance at the compensated harmonic frequencies since the desired gain at the desired phase cannot be obtained with virtual impedance given by (11).

### *B. Improved Capacitive Virtual Impedance Loop*

Instead of using an integrator to represent the virtual capacitive impedance as was performed in [8], a PI compensator was used to allow control over the magnitude and phase at the $n^{th}$ harmonic frequency. The virtual impedance transfer function can therefore be defined as follows:

$$\begin{aligned} Z_d(s) &= R_V - \sum_{h=3,5,7,9} \left(\frac{\omega_{ch}}{s^2 + \omega_{ch} s + \omega_h^2}\right)\left(\frac{k_{ph}s + k_{ih}}{s}\right) \\ &= R_V - \sum_{h=3,5,7,9} \frac{\omega_{ch}(k_{ph}s + k_{ih})}{s^2 + \omega_{ch} s + \omega_h^2} \end{aligned} \tag{16}$$

where $k_{ph}$ are the proportional gains and $k_{ih}$ are the integral gains. Assuming that the bandwidth $\omega_{ch}$ at the $n^{th}$ harmonic frequency is determined such that the interaction with the

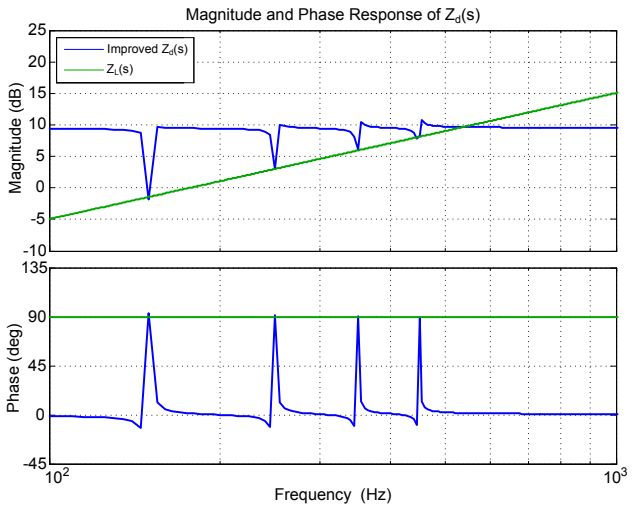



Fig. 8. Magnitude and phase response of the proposed virtual impedance transfer function $Z_d$(s) vs. the inductive grid side impedance $Z_L$(s) where $R_V = k_{ph} = 3\Omega$, $k_{ih} = |Z_L(\omega)|_{\omega=\omega_h}$, $\omega_{ch} = \frac{0.02\omega_h}{h}$ and $L_2 = 0.9mH$ is the grid side inductance.

adjacent harmonics is negligible, then the magnitude and phase contribution of $Z_d$(s) at each of the $n^{th}$ harmonic frequencies can be designed by considering the effect of each harmonic separately to determine the controller gains and then substituting in (16). $Z_d$(s) at the $n^{th}$ harmonic can be denoted by:

$$Z_d(s) = R_V - \frac{\omega_{ch}(k_{ph}s + k_{ih})}{s^2 + \omega_{ch}s + \omega_h^2} \tag{17}$$

Substituting for s = j$\omega$ in (16):

$$Z_d(\omega) = \frac{j\omega\omega_{ch}(R_V - k_{ph}) + (\omega_h^2 R_V - \omega_{ch}k_{ih} - R_V\omega^2)}{j\omega\omega_{ch} + (\omega_h^2 - \omega^2)} \tag{18}$$

The gains $k_{ph}$ and $k_{ih}$ can be determined from the $|Z_d(\omega)|_{\omega=\omega_h}$ and $\angle Z_d(\omega)_{\omega=\omega_h}$ of (9) at $\omega = \omega_h$ given by:

$$|Z_d(\omega)|_{\omega=\omega_h} = \frac{\sqrt{(\omega_h R_V - \omega_h k_{ph})^2 + k_{ih}^2}}{\omega_h} \tag{19}$$

$$\angle Z_d(\omega)_{\omega=\omega_h} = \tan^{-1}\left(\frac{-\omega_h(R_V - k_{ph})}{k_{ih}}\right) - 90^o \tag{20}$$

Hence from (20), to obtain the required phase of $90^o$ at the $n^{th}$ harmonic, the proportional gain $k_{ph} = R_V$. To match $|Z_d(\omega)|$ with the required inductive impedance magnitude $|Z_L(\omega)|$ at $\omega = \omega_h$ then from (19), $k_{ih} = |Z_L(\omega)|\,\omega_h$. One may note that when $R_V = 0$ then (16) reduces to (7) such that $k_{ih} \equiv k_{Ch}$.

The magnitude and phase response of $Z_d(s)$ for the proposed capacitive virtual impedance is shown in Fig. 8. By using the PI compensator, magnitudes equal to those of the grid side inductance $Z_L(s)$ at the compensated harmonic frequencies of $Z_d(s)$ were obtained. The phase at these frequencies was also of $90^o$ as required to cancel the effect of the inductive voltage drop across the grid side inductor.

## IV. Simulation Results

The aim of this section is to verify the effectiveness of the improved virtual impedance loop being proposed in reducing the voltage harmonics at the PCC. The two inverters, were connected sequentially to the microgrid while operating in islanded mode. Inverter 1 is connected at t=0 and sets the microgrid voltage and frequency according to the droop control. It is assumed that each inverter can handle the load present on the microgrid. Inverter 2 is connected to the microgrid after it is synchronized with the microgrid voltage. Under these conditions, it is expected that the inverters share equally the active and reactive power demanded by the load. The simulation model parameters are given in Table I.

The microsource inverters were required to supply a local single phase rectifier with smoothing capacitor ($L_p = 84\mu H$, $C_p = 235\mu F$ and $R_p = 100\Omega$). The voltage harmonics that were measured at the PCC with and without the capacitive virtual impedance of (16) with only inverter 1 connected to the microgrid are shown in Fig. 9. The voltage THD without compensation was of 5.55% while this was reduced to 4.8% when $Z_d(s)$ was added to the primary control loops. Fig. 10 compares the voltage harmonics at the PCC for the simulations that were carried out with and without the capacitive virtual impedance (16) with both inverters connected to the microgrid.

TABLE I
Simulation Model Parameters for the Inverters Connected to the Microgrid.

| Inverter | Inverter Filter Parameters | | | | | |
|---|---|---|---|---|---|---|
| | $R_1$ | $L_1$ | $C_1$ | $R_2$ | $L_2$ | $R_d$ |
| | $\Omega$ | $mH$ | $\mu F$ | $\Omega$ | $mH$ | $\Omega$ |
| 1 | 0.040 | 3.60 | 25.0 | 0.010 | 0.90 | 2 |
| 2 | 0.032 | 2.80 | 20.0 | 0.008 | 0.72 | 2 |

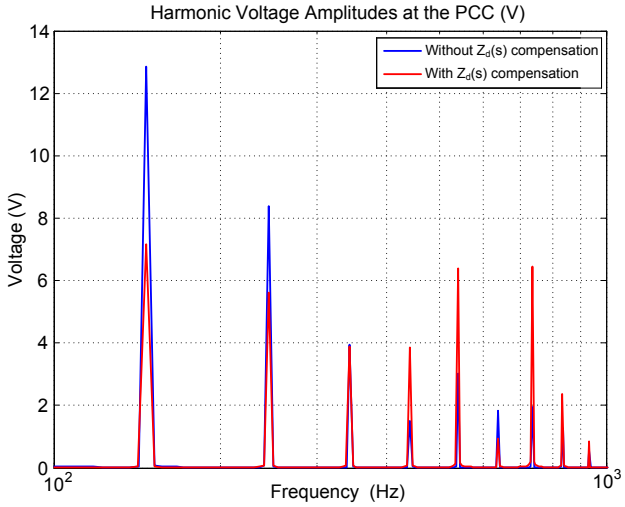



Fig. 9. Voltage harmonics at the PCC for the single phase rectifier with smoothing capacitor load ($L_p = 84\mu H$, $C_p = 235\mu F$ and $R_p = 100\Omega$) with only inverter 1 connected to the microgrid.

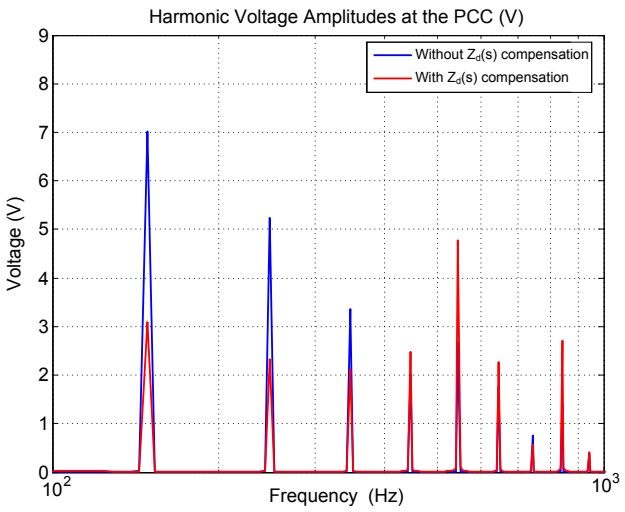



Fig. 10. Voltage harmonics at the PCC for the single phase rectifier with smoothing capacitor load ($L_p = 84\mu H$, $C_p = 235\mu F$ and $R_p = 100\Omega$) when both inverters are connected to the microgrid.

The voltage harmonics at the PCC are reduced due to the addition of another inverter since the inverters share the load current thereby reducing the voltage drop across the grid side inductance. The voltage THD without compensation was of 3.36% while this was reduced to 2.57% when $Z_d(s)$ was added to the primary control loops of both inverters.

Hence, when the capacitive virtual impedance was introduced into the inverter primary contol loops, a 15% reduction in THD was observed for the case of a single inverter and a 31% reduction was observed when two inverters where connected to the microgrid. Therefore, these simulation results verify the effectiveness of the capacitive virtual impedance loop in improving the voltage THD at the PCC. One should point out that the harmonics cannot be completely eliminated from the PCC for the considered setup since the harmonic voltage vector that is generated by the virtual capacitance loop depends on the magnitude of the harmonic current flowing. However, with the proposed loop the harmonic content becomes distributed such that the voltage harmonic distortion is improved.

## V. Conclusion

This paper analyses the performance of the basic capacitive virtual impedance loop to improve the harmonic distortion at the PCC when the inverters operate as an island. Virtual resistances added to improve the stability of the inverters connected to microgrid compromise the operation of this compensation loop. Hence, the virtual impedance loops were redesigned to provide the required compensation even when the virtual resistance was present. Simulation results have shown that the proposed loop achieved a significant reduction in the THD at the PCC, even though a virtual resistance was used, thereby indicating the effectiveness of the proposed algorithm to dampen the voltage harmonics.

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